



Software Defined Radio (SDR) Development Platform Request for Information (RFI)

**Issued by:
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RFI Number: SCAT-RFI-003-09

Version 1.1

Issue Date: 9/14/2009

Respond to: dmurotak@scatechnica.com

Requested Response Date: 10/15/2009

Change Notice: Changes from Version 1.0 are marked with change bars in the margin. Requirements RF12, RF17-20 and OP02 have been changed. The respond-by date has been extended to 10/15/2009.

Note: This is not a solicitation to purchase equipment, software or intellectual property. No reimbursement is offered for responses to this RFI. If a proprietary response will be made, please contact SCA Technica, Inc. (the "Company") to initiate a Non Disclosure Agreement. This is strictly a request for information conducted by SCA Technica, Inc. to determine the availability, capabilities and cost for commercial on-the-shelf (COTS) radio test bed and prototyping equipment consisting of software/firmware reconfigurable radio hardware, software, and rapid prototyping tool chains, for the purpose of research and development in software defined radio, cognitive radio and mobile ad-hoc networks (MANET) by the Company or its customers, which may include, but is not limited to, the United States Government. Any responses received by the Company will only be used for internal purposes, unless a Release has been first solicited and received by the Company from the Respondent permitting the information to be provided to Third Parties.

1. Introduction and Scope:

SCA Technica, Inc. (the Company) is conducting a trade study to determine the availability, capabilities and costs for commercial, small form factor, on-the-shelf (COTS) radio test bed and prototyping equipment consisting of software/firmware reconfigurable radio hardware and software, and rapid prototyping tool chains, for the purpose of research and development in software defined radio (SDR), cognitive radio (CR) and mobile ad-hoc networks (MANET). The Company performs on prime contracts with the United States Government and subcontracts with commercial companies in the United States and abroad, which require the testing of SDR, CR and MANET software and radio “signals in space”. The latter tests are primarily for the validation of software “waveforms” to determine their interoperability with legacy radio sets.

- The Company employs a SCA tool chain based on Zeligsoft CE™ and Zeligsoft CG™.
- The Company employs SCA compliance test software called JTRS Test Application Program (JTAP), provided by the United States Government.
- The Company employs a software tool chain based on:
 - i. Mathworks™ MATLAB™ and SIMULINK™ modeling tools to develop cores for Altera and Xilinx target platforms. This is a MATLAB m-file and SIMULINK based tool chain capable of producing highly optimized Altera and Xilinx cores based on a vendor library.
 - ii. Celoxica DK Design Suite for Xilinx target platforms. This is a Handel C-based tool set capable of producing highly optimized Xilinx cores based on a vendor library.

The company requests information on COTS RF/IF and baseband SDR platforms which employ open architecture hardware and software, Altera PLDs or Xilinx FPGAs and “hard” general purpose processor (GPP) cores with hardware memory management units (such as the PowerPC) capable of supporting a Joint Tactical Radio System (JTRS) Software Communication Architecture¹ (SCA 2.2.2) and “public” application programming interfaces (API). Additionally, a second GPP hard core is desired for security functions.

2. System Requirements

2.a. Radio Frequency (RF):

- RF01: Transmit/Receive Frequency: As a minimum, the system shall support RF transmitted and received signals in the range of 1200-2400 MHz. As an objective, the system shall support RF transmitted and received signals in the range of 225-2600 MHz.
- RF02: Transmit/Receive Channel: As a minimum, the system shall support 25 KHz narrowband channels. As an objective, the system shall support wideband signals up to 20 MHz, and also be selectable to 25 KHz narrowband signals.
- RF03: Number of Channels: As a minimum, the system shall support one true half-duplex transmit/receive channel, with receive and transmit channels independently selectable (F1/F2). Optionally, the system shall support two true half-duplex channels. If two channels are provided, the RF systems shall support coherent reception to support two-channel beamforming.
- RF04: Frequency Diversity: The F1/F2 half-duplex shall be selectable ON (F1/F2) or OFF (F1/F1).

¹ SCA version 2.2.2, Annex B (Application Environment Profile)

- RF05: Occupied Bandwidth: When supporting 25 KHz narrowband signals, the receiver shall support an occupied bandwidth of at least 2.0 MHz in its narrowband mode.
- RF06: Switching Time: TBD.
- RF07: Receiver Sensitivity: Shall be at least -103 dBm.
- RF08: Receiver gain at sensitivity: Shall be at least 110 dB.
- RF09: Receiver Dynamic Range: Shall be at least 90 dB.
- RF10: Receiver Carrier to Noise Ratio: Shall be at least 3.1 dB.
- RF11: Receiver Eb/N0: Shall be at least 5 dB.
- RF12: Receiver Noise Figure: Shall be less than 10 dB².
- RF13: Receiver Third Order Intercept Point: Shall be at least 1 dBm.
- RF14: Receiver Second Order Intercept Point: Shall be at least 39 dBm.
- RF15: Receiver Wideband Phase Noise: Shall be less than -136 dBm.
- RF16: Analog vs Digital: The RF transceiver(s) may employ analog up-converters and down-converters. If an Intermediate Frequency (IF) stage is used, please identify the RF/IF interface characteristics (e.g. frequency, bandwidth, physical interface connector specifications if any, etc.). If superheterodyne receiver designs are used, please specify whether a single, double or triple conversion design is employed, and identify the frequency plan (local oscillator frequencies).
- RF17: Transmit Power: Shall be adjustable over a wide range from 0 to +10 dBm.
- RF18: Transmitter Second Harmonic Attenuation: Shall be at least 40 dBc.
- RF19: Transmitter Third Harmonic Attenuation: Shall be at least 40 dBc.
- RF20: Transmitter Other Harmonic Attenuation: Shall be at least 60 dBc.
- RF21: Transmitter Frequency Tolerance: Shall be less than +/- 20 ppm.
- RF22: Transmitter 99% Power Bandwidth: In narrowband mode, shall be less than 1.8 MHz.
- RF21: RF Pre-selector(s): Not required. If a product is optionally available, please provide specifications and cost. In particular, please indicate how the pre-selector is tuned by the SDR, and what are its performance characteristics? Also, please indicate if an industry standard RF pre-selector control API is employed, if any.
- RF22: Antenna Interface: Any industry standard RF connector may be supplied (please specify). Also, for multi-frequency operation, please specify the antenna tuning control API employed, if any.
- RF23: Diplexer(s): Not required. If an optional tunable diplexer is available, please provide specifications and cost. In particular, how is the diplexer tuned by the SDR, and what are its performance characteristics? Also specify the diplexer control API employed, if any.

2.b. Intermediate Frequency (IF).

- IF01: Analog vs Digital: The IF upconverters and downconverters, if used, may be analog or digital.
- IF02: Occupied Bandwidth (99%): Shall be at least 2.0 MHz in narrowband mode. If wideband mode is supported, it shall be at least 20.0 MHz.
- IF03: Analog to Digital Conversion: Analog to digital conversion (ADC) and digital to analog conversion (DAC) shall be supplied at the baseband interface. As a minimum, the

² This requirement assumes a 3 dB insertion loss for an optional pre-selector. In combination with a pre-selector, the overall requirement is 7 dB.

ADC and DAC shall support 14 bit sampling at 4 megasamples per second³ in narrowband mode, or 8 bit sampling at 40 megasamples per second⁴ in wideband mode.

- IF04: RF/IF Connectors: If a separate IF module is supplied, industry standard RF connectors shall be employed to connect the RF and IF modules.
- IF05: IF/Baseband Connectors: Industry standard digital interfaces and connectors, such as Ethernet or USB shall be used to connect the RF/IF module to the baseband digital interface.

2.c. Baseband digital signal processing.

- DSP01: FPGA: Each channel DSP module shall support either an Altera programmable logic device (PLD)⁵ or a Xilinx field programmable gate array (FPGA)⁶, hereafter referred to generically as “FPGA”.
- DSP02: Logic Elements: Each channel FPGA shall contain a minimum of 80,000 (80K) logic elements, not including either a hard GPP “core” or reconfigurable elements to be used to provide a GPP core with a memory management unit.
- DSP03: Data Bandwidth: The channel DSP module shall support a minimum of 320 Mb/s data, bidirectional, at the interface to the RF/IF ADC and DAC.
- DSP04: GPP Interface: The channel DSP module shall support an industry standard digital interface to at least one external GPP⁷.
- DSP05: Two channel: The system shall provide a minimum of two channel DSP modules.
- DSP06: Clocking: The DSP modules shall be capable of being coherently clocked using an external timing reference.
- DSP07: Open Architecture: As an objective, channel DSP modules shall employ an open industry standard interface⁸.
- DSP07: Non Blocking Data Fabric: A separate non-blocking, low latency high speed data interface shall be employed for the data connection between channel DSP module(s) and the baseband ADC/DAC interface. The data base shall be separate from either the GPP memory bus, or the general purpose control bus.

2.d. General purpose processor.

- GPP01: BSP: The GPP shall have a board support package (BSP) to support a high assurance COTS real time operating system, such as Green Hills Software (GHS) Integrity, or Wind River VXWorks. Optionally, the GPP shall have a BSP supporting AEP POSIX compliant Linux.
- GPP02: MMU: The GPP shall employ a memory management unit (MMU) implemented in hardware, sufficient to support a RTOS separation kernel employed in high assurance RTOS, such as DO-178B or MILS certified RTOS.
- GPP03: RAM: The GPP shall contain a minimum of 64 megabytes (MB) random access memory (RAM). As an objective, the RAM shall be expandable to a minimum of 512 MB. Industry standard, replaceable memory modules should be employed.

³ 2x oversample at 2 MHz. At 14 bits per sample, this generates a 56 Mb/s data stream per channel at the baseband interface.

⁴ 2x oversample at 20 MHz. At 8 bits per sample, this generates a 320 Mb/s data stream per channel at the baseband interface.

⁵ Cyclone II/III preferred.

⁶ Virtex 4/5 preferred.

⁷ An external GPP is one which is not embedded in the FPGA used by the channel modem.

⁸ Examples are stackable PC-104 and PCI mezzanine “daughter board” connectors.

- GPP04: Embedded GPP: The GPP may be embedded within the FPGA, either as a hard core or as a core employing reconfigurable logic modules⁹, or it may be separate from the FPGA.
- GPP05: Ethernet and USB 2.0 Interfaces: As a minimum, the GPP shall support at least one 100/1000 BT Ethernet interface and at least two USB 2.0 interfaces.
- GPP06: GPS Interface: As a minimum, the GPP shall support at least one GPS interface¹⁰.
- GPP07: SCA Compatible: At least one GPP shall be capable of supporting the JTRS SCA compatible operating environment (OE) including an RTOS, an object request broker (ORB), a SCA Core Framework (CF), and the JTRS Public SCA 2.2.2 APIs¹¹.

2.e. Operational and Form Factor Requirements:

OP01: Transportable: The equipment shall be transportable and rack mountable for the purpose of supporting on-the-move testing, such as vehicular or flight testing.

OP02: Form Factor: The equipment modules shall be an industry standard small form factor¹². The equipment shall be capable of rack mounting in a 19" rack chassis. The use of adapters is permitted.

OP03: Power Supply: The equipment shall be capable of being powered using 110-120V AC power as a minimum. Optional 12 or 24 volt DC power supplies, to support mobile or airborne flight tests, is also desired.

OP04: Cooling: The equipment shall be capable of sustained operation at up to 10,000 feet altitude without external cooling or pressurization.

3. Other Instructions:

When responding, please include the following information:

- a. A description of the product, including to what extent it satisfies the requirements. If minimum requirements are not met, please identify those requirements, and address how the shortcomings might be resolved.
- b. Unit Pricing. Please include a break-out of license costs for the system including operating environment, board support or development tools.
- c. Time to delivery, after receipt of order.
- d. Availability of full-MIL or industrial "rugged" components and modules.
- e. Ease with which the product can be transitioned into a "production" embedded radio system for rugged commercial or military production.
- f. Any previous utilization of the equipment in ground mobile or airborne applications.
- g. Exportability (outside the USA).

⁹ An example is the PowerPC core(s) embedded in the Virtex 4/5 FPGAs.

¹⁰ An example is NMEA protocol using serial RS-232 or USB 2.0 physical connections.

¹¹ A minimum example is OSSIE or SCARI-OPEN CF, Omni ORB, and real time Linux OS.

¹² Examples include PC-104 or 3U cPCI.